	Technical Sessions								
Sessio	n I		Session II						
S.No.	Papei	Authors, Title	Paper	Authors, Title					
	ID		ID						
1	131	Ambika Prasad Shah, Amirhossein Moshrefi and Michael Waltl, Utilizing NBTI for operation detection of Integrated Circuits	41	Mohammad Asan Basiri M, Asynchronous Hardware Design for Floating Point Multiply-Accumulate Circuit					
2	14	Javed Gaggatur and Abhishek Chaturvedi, A 1.25-20 GHz wide Tuning Range Frequency Synthesis for 40Gb/s SerDes Application	56	Chandan Das, Sarit Chakraborty and Susanta Chakraborty, An Efficient Test and Fault Tolerance Technique for Paper- Based Digital Microfluidic Biochips					
3	27	Bandan Bhoi, Neeraj Kumar Mishra, Shailesh Singh Chauhan and Sarthak Acharya, Analyzing design Parameter of Nano -Magnetic Technology Based Converter Circuit	65	Amarya Dutta, Riya Majumder, Debasis Dhal and Rajat Kumar Pal, A Generalized Technique of Automated Pin Sharing on Hexagonal Electrode based Digital Microfluidic Biochip along with its Design Methodology					
4	36	Debanjana Dutta, Sweta Agarwal, Vikas Kumar, Mayank Raj, Baidyanath Ray and Ayan Banerjee, Design of Current Mode Sigmoid Function and Hyperbolic Tangent Function	76	Jyotiranjan Swain and Sumanta Pyne, A Space Efficient Greedy Droplet Routing for Digital Microfluidic Biochip					
5	39	Mohammad Asan Basiri M, Flexible Adaptive FIR Filter Designs Using LMS Algorithm	78	Aditya Kumar Hota and Kabiraj Sethi, Design of 635 MHz Bandpass Filter using High-Q Floating Active Inductor					
Sessio	n III		Session	Session IV					
1	89	Sounak Roy and M. Mahendra Reddy, Clock Pulse based Foreground Calibration of a Sub-Radix-2 Successive Approximation Register ADC	120	Purvi Agarwal, Ananya Garg, Ruchi Dhamnani, Shrivisal Tripathi and Manoj Kumar Majumder, An Efficient Wireless Charging Technique using Inductive and Resonant Circuits					
2	94	Priyanka Panigrahi, Rajesh Kumar Jha and Chandan Karfa, User Guided Register Manipulation in Digital Circuits		Archana S and Bhaskar M., A 2.4 GHz High Efficiency Capacitive Cross coupled Common Gate Class-E Differential Power Amplifier.					
3	103	Moumita Acharya, Samik Basu, Biranchi Narayan Behera and Amlan Chakraborty, Approximate Computing Based Adder Design for DWT Application	151	Raviteja Kammari and Vijaya Sankara Rao Pasupureddi A Widely Linear, Power Efficient, Charge Controlled Delay Element for Multi-Phase Clock Generation in 1.2V, 65nm CMOS					
Session V			Session VI						
1	164	Sunanda Ambulker, Jitendra Kumar Mishra and Sangeeta Nakhate, A CMOS low Noise Amplifier with Improved gain	7	Kanika Monga and Nitin Chaturvedi, A CMOS/MJT based Novel Non-Volatile SRAM cell with Asynchronous Write Termination for Normally OFF Applications					
2	174	Sayantani Roy, Debesh Das and Arighna Deb, Delay Efficient all Optical carry lookahead adder	156	Neha Gupta, Tanisha Gupta, Sajid Khan,Gunjan Rajput and Santosh Kumar Vishvakarma, Low Leakage Highly Stable Robust Ultra Low Power 8T SRAM Cell					
3	35	Deepthi Amuru, Andleeb Zahra and Zia Abbas, Statistical Variation aware Leakage and Total Power Estimation in 16nm VLSI Digital Circuits based on Regression Models	142	Neha Gupta, Jitesh Prasad, Rana Sagar Kumar, Abhinav Vishwakarma and S. K. Vishvakarma, A Robust Low Power Write-Assist Data-Dependent-Power-Supplied 12T SRAM Cell					
Sessio	n VII		Session	Session VIII					
1	42	Shivendra Singh Parihar and Ramchandra Gurjar, Compact Modeling of Drain Extended MOS Transistor using BSIM-BULK Model		Ankur Beohar, and Santosh Kumar Vishvakarma, Compact Spiking Neural Network System with SiGe based Cylindrical Tunneling Transistor for Low Power Applications					

2	110	Shivendra Yadav, Chithraja Rajan, Dheera Sharma and Sanjay	133	Shanti Rekha Shanmugham and Saravanan Paramasivam,
		Balotiya, GaAs-SiGe based novel device structure of doping less Tunnel FET		Threshold Implementation of a low cost CLEFIA-128 clipper for Power Analysis Attack resistance
3	180	Shagun Pal and Brijesh Kumar, Low Voltage Dual-Gate Organic Thin Film transistors with Distinctly Placed Source and Drain	16	Raghunath K P, Manu Sagar K V, Gokulan T, Kundan Kumar and Chetan Singh Thakur, ASIC based LVDT Signal Conditioner for High-Accuracy measurements
4	106	Harshit Goyal and Vishwani Agrawal, Technology Characterization Model and Scaling for Energy Management	58	Neelam Arya, Anil Kumar Rajput, Manisha Pattanaik and G.K. Sharma, Quality Driven Energy Aware Approximated Core Transform Architecture of HEVC Standard
5	117	Niramal Kumar Boran, Dinesh Kumar Yadav and Rishabh Iyer, Performance modeling and Dynamic Scheduling on Heterogeneous-ISA multi core Architecture	68	Vineesh Vs, Jay Adhaduknand Binod Kumar, Identification of Effective Guidance Hints for Better Design Debugging by Formal Methods
Sessi	on IX			Session X
1	81	Yadukrishnan Mekkattillam, Satyajit Mohapatra and Nihar Ranjan Mohapatra, The Design and Calibration of 14 Bit 10 kS/s Low Power SAR ADC for Biomedical Applications	102	Govind Bajpai, Aniket Gupta and Nitanshu Chauhan, Real Time Implantation of Convolutional Neural Network to Detect Plant Diseases using Internet of Thing
2	87	Veda Bhanu P, Pranav Venkatesh Kulkarni, et.al., Multi-Application based Fault-Tolerant Network-on-Chip Design for Mesh Topology using Reconfigurable Architecture	108	Saurabh Gangurde and Binod Kumar, A Unified methodology for Hardware obfuscation and IP watermarking
3	98	Aneesh Ravindran, Sandra Jean, Mervin J, Vivian Desalphine and David Selvakumar, RISC-V Half Precision Floating Point Instruction Set extension and Co-processor	118	Lakshmi Manasa Sistla and Lakshmi Narayanan G, A Latency and Throughput Efficient Successive Cancellation(SC) Decoding of Polar Codes
4	70	Piyush Tankwal, Vikas Nehra and Brajesh Kumar Kaushik, Comparative Analysis of Logic Gates Based on Spin Transfer Torque (STT) and Differential Spin Hall Effect (DSHE) Switching Mechanisms	121	Swatilekha Majumder, A Novel Gate-level On-Chip Crosstalk Noise Reduction Circuit for Deep Sub-micron Technology
5	99	Aneesh Ravindran, Vinay Kumar, Vivian Desalphine and David Selvakumar, Functional Simulation Verification of RISC-V Instruction Set based High Level Language Modeled FPU	123	Arun Mohan, Saroj Mondal and Surya Shankar Dan., On-Chip Threshold Compensated Voltage Doubler for RF Energy Harvesting
Session XI				Session XII
1	127	Ankur Pokhara, Biswajit Mishra and Purvi Patel., All-Digital CMOS On-Chip Temperature Sensor with Time-Assisted Analytical Model	141	Sajid Khan, Neha Gupta, Abhinav Vishvakarma, Shailesh Singh Chouhan, Jai Gopal Pandey and Santosh Vishvakarma, Dual-Edge Triggered Light Weight Implementation of AES for IoT Security
2	169	Shah Zahid Yousuf, Anil Kumar Bhardwaj and Rohit Sharma, Investigating the Role of Parasitic Resistance in a Class of Nanoscale Interconnects	168	Rajul Bansal and Abhijit Karmakar, Efficient closely-coupled integration of AES coprocessor with LEON3 processor
3	137	Devika R Nair and Purushothaman, A Brain Inspired One Shot Learning Method For High Dimensional Computing	181	Priyamvada Sharma and Bishnu Prasad Das, A True Single- phase Error Masking Flip-Flop with Reduced Clock Power for Near-Threshold Designs
4	143	Rose George Kunthara, Neethu K, Rekha K James, Simi Zerine Sleeba, Tripti S Warrier and John Jose, 2L-2D Routing for Buffered Mesh Network- on-Chip		
5	152	Gopal Raut, Vishal Bhartiy, Gunjan Rajput, Sajid Khan and Santosh Kumar Vishvakarma, Efficient Low Precision CORDIC algorithm for Hardware Implementation of Artificial Neural Network		

S.No.	Poster Paper						
	Paper ID Authors, Title						
1	2	Varun Kumar Dwivedi, Madhvi Sharma and Chandaka Venu, Automations and Methodologies for efficient and quality conscious analog layout implementation					
2	60	V.Jeffry Louis and Jai Gopal Pandey, A Novel Design of SRAM using Memristors at 45 nm Technology					
3	85	Saroja Siddamal, Suhas Shirol, Shraddha Hiremath and Nalini Iyer, Design and Physical Implementation of Mixed Signal Elapsed Time Counter in 0.18µm CMOS Technology					
4	92	Bappaditya Mondal, Anirban Bhattacharjee, Shubham Saha, Shalini Pareskh, Chandan Bandyopadhyay and Hafizur Rahaman, An Approach for Detection of Node Displacement Fault (NDF) in Reversible Circuit					
5	93	Mrinal Goswami, Mayukh Ray and Bibhash Sen, A Realistic Configurable Level Triggered Flip Flop in Quantum-dot Cellular Automata					
6	116	Rajeev Ranjan Silmana, Abraham T Mathew and Sumitra Singh, Design and Simulation of different Microfluidic Channel Designs					
7	154	Sajid Khan, Neha Gupta, Gopal Raut, Gunjan Rajput, Jai Gopal Pandey and Santosh Vishvakarma, An Ultra Low Power AES Architecture for IoT					
8	177	Venketa Appa Rao Yempada and Srivatsava Jandhyala, Simulation study of III-V Lateral Tunnel FETs with Gate-Drain Underlap					
9	129	Deven Patanvariya, Sudhan Kumar and Lalat Indu Giri, Influence of Current Collapse in AlGaN/GaN High Electron Mobility transistors					
10	132	Vijay Rao Kumbhare, Punya Prasanna Paltani and Manoj Kumar Majumder, Novel Approach for Improved Signal Integrity and Power Dissipation using MLGNR Interconnects					
11	165	Avinash Verma and Gaurav Kaushal, Radiation Hardened By Design Sense Amplifier					